Remarks/Arguments

Applicant has received and carefully reviewed the Office Action mailed May 8, 2003. Claims 1-34 remain pending. Reexamination and reconsideration are respectfully requested.

In paragraph 1 of the Office Action, the Examiner objected to the drawings because the arrows on Figures 6-15 should be identified. The undersigned discussed this objection with the Examiner on July 31, 2003. The Examiner indicated that a number of arrows appeared to be missing from these Figures. In response, Figures 6-15 were amended to include the arrows requested by the Examiner. Annotated sheets showing the changes to Figures 6-15 are enclosed for the Examiner's approval.

In paragraph 2 of the Office Action, the Examiner objected to the abstract because at page 1, line 5, the Serial Number of the related U.S. Patent Application is missing. It appears that the Examiner inadvertently referenced the Abstract in paragraph 2 of the Office Action, but meant to object to page 1 of the specification. In any event, page 1, line 5 of the specification has been amended to include the Serial Number of the related U.S. Patent Application.

In paragraph 4 of the Office Action, the Examiner rejected claims 1, 23-25, 28, 33 and 34 under 35 U.S.C. § 102(e) as being anticipated by Varadarajan et al. (U.S. Patent No. 5,838,583). The Examiner states that Varadarajan et al. suggests selecting one of the nets via a user input (citing column 15, lines 26-27, 38-39; and Figure 2a); identifying selected leaf cells that are connected to the selected net (citing column 26, line 7 and Figure 2a); and selecting the identified leaf cells using a standard cell placer (170) as shown in Figure 1).

After careful review, Applicants must respectfully disagree. As noted in the present specification, and to give a little background:

> To date, selecting cells that are connected to a net or group of nets has been difficult. For example, to select cells that are connected to a particular net, the circuit designer typically must manually find each instance name by scanning some external printout, panning through a list of instance names or net names in the physical window, or by identifying the physical representation of the cell within the floorplanning window. Each of these have proven to be time consuming and tedious, particularly since many logic design synthesis software programs assign computer generated component and net names.
>
> As a result of these difficulties, circuit designers often only have time to manually place a fraction of the cells within a data path. The remaining cells are placed using automatic placement tools, which typically use algorithms that optimize wire congestion rather than performance or gate density. Accordingly, any improvement in the manual placement process that can significantly reduce the time required to identify, select and align cells associated with a net or group of nets within a circuit design would be beneficial.

(Specification, page 10, lines 1-14). Claim 1 recites:

> 1. (Original) A computerized method for selecting cells in a circuit design database, the circuit design database having one or more levels of hierarchy including one or more logic functions composed of one or more other logic functions and/or one or more leaf cells, the leaf cells forming the lowest level of hierarchy in the circuit design database, each of the leaf cells having one or more inputs and one or more outputs, the circuit design database having one or more nets, each of the nets for connecting an output port of a source leaf cell to an input port of one or more destination leaf cells, the computerized method comprising the steps of:
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> selecting one of the nets via a user input device;
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> identifying selected leaf cells that are connected to the selected net; and
>
> selecting the identified leaf cells.

(Emphasis Added) As can be seen, claim 1 recites a method of selecting one of the nets via a user input device; identifying selected leaf cells that are connected to the selected net; and selecting the identified leaf cells. As can be seen, such a method may,

for example, help a circuit designer interactively select cells that are connected to a net or group of nets.

In contrast to the foregoing, Varadarajan et al. appears to relate to a more automated way of optimizing placement and routing of data paths. In Varadarajan et al., a number of tile files are created for each datapath function. The tile files appear to be created in advance by a designer. According to Varadarajan et al., a tile file is a structured description of a datapath function, describing the relative vertical and horizontal placement of all logic cell instances within the datapath function (Varadarajan et al., abstract; see also Figure 5 of Varadarajan et al.). Varadarajan et al. state that there is one tile file for each unique datapath function, and the datapath function instances are associated with a particular tile file by a tile file list file (Varadarajan et al., abstract). Varadarajan et al. further state:

> The datapath floorplanner uses the tile files to integrate the placement information with the specific function instances, and further allows the specification of clusters, function interleaving, and net side constraints per region. A datapath placer places the datapath functions in each region using the relative placement information and constraints. The routing space estimator estimates the space needed for routing a placed region. All of this information is interactively provided to the circuit designer so as to allow almost real time modification of datapath placement.

(Emphasis Added)(Varadarajan et al., abstract).

In paragraph 4 of the Office Action, the Examiner cites to column 15, lines 26-27, 38-39; and Figure 2a of Varadarajan et al. as suggesting the step of selecting one of the nets via a user input. Applicants would like to point out that column 15, lines 26-27 and 38-39 of Varadarajan et al. relate to a process for specifying "Net Exit Constraints" for a datapath region. More specifically, column 15, lines 11-40 of Varadarajan et al. state:

> The process of specifying net exit constraints, for a current datapath region 303 may be described as follows:
> 1. Determine nets that exit the datapath region 303.
> 2. For each logic cell instance in the netlist or layout database 195.
> 3. Traverse nets that couple the instance to one or more, terminating instance.
> 4. Determine for each terminating instance whether its parent datapath region 303 is the current datapath region 303, and if not, mark the net as an exiting net.
> 5. For each exiting net, assign a default exit value. The default values are one of (Top, Bottom, Left, Right). They are heuristically assigned, and accordingly, may be overridden by the circuit designer.
> 6. Identify control net as nets that connect multiple instances within a function.
> 7. Assign default as Top or Bottom, depending on position of current datapath region relative to other datapath regions.
> 8. Identify datapath nets, as nets that connect instances in multiple functions. If pin instance data is available for net, use the location of pin to determine net exit, otherwise, assign default as Right or Left depending on position of current datapath region relative to other datapath regions.
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> The resulting nets are displayed to the circuit designer on the display device. The circuit designer may choose to modify any or all of the default net exit assignments.

The portions of Varadarajan et al. cited by the Examiner are underlined above. Nothing in this process appears to suggest the step of selecting one of the nets via a user input device, as recited in claim 1. Instead, the recited process appears to be performed by a computer. Furthermore, nothing in this process appears to suggest the steps of identifying selected leaf cells that are connected to the selected net, or selecting the identified leaf cells, as recited in claim 1. Instead, the recited process appears to be concerned with specifying net exit constraints for a datapath region.

The Examiner also cites to column 26, line 7 of Varadarajan et al., which is a portion of claim 1, as suggesting the step of identifying leaf cells that are connected to the

selected net. Column 26, line 7 of Varadarajan et al. recites "i) an instance identifier specifying a logic cell instance". However, as can readily be seen by examining the rest of claim 1, this merely relates to an instance identifier (e.g. a name) that is part of a first structured description of the unique relative vertical or horizontal placement of logic cell instances in a datapath function. Applicants do not see how this relates to selecting identified leaf cells, and more particularly, selecting those leaf cells that are identified as being connected to a selected net, wherein the selected net is selected by a user input device. In view of the foregoing, claim 1 is believed to be clearly patentable over Varadarajan et al. For similar and other reasons, independent claims 23 and 33, and dependent claims 24-25, 28 and 34, are also believed to be clearly patentable over Varadarajan et al.

In paragraph 7 of the Office Action, the Examiner rejected claims 2-6, 15-17, 19, 20, 26 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Varadarajan et al. as applied to claims 1, 23 and 33 above, in view of Aubel et al. Since independent claims 1, 23 and 33 are believed to be clearly patentable over Varadarajan et al., dependent claims 2-6, 15-17, 19, 20, 26 and 27 are also believed to be clearly in condition for allowance. Aubel et al. does not appear to help overcome the deficiencies in Varadarajan et al.

In addition, dependent claims 2-6, 15-17, 19, 20, 26 and 27 are believed to recite additional elements that render them independently patentable over Varadarajan et al., and/or Varadarajan et al. in view of Aubel et al.

Specifically with respect to Aubel et al., the "source" and "target" leaf cells mentioned by the Examiner in paragraph 7 of the Office Action are not necessarily source

leaf cells that provide signals to target leaf cell via nets, as the Examiner appears to be suggesting. Rather, Aubel et al. state:

> The method comprises the steps of setting an orientation mode indicating the orientation of physical placement of a logic function or cell. The orientation mode includes selecting the reflection of the physical placement of a logic function or cell about the horizontal axis, about the vertical axis, or about both the horizontal and vertical axes. A first set of nodes (the "source" set) from the logic design hierarchy is selected. The first set of nodes is usually already placed in the floor plan or previously stored in a logic function design database. However, it is not required that all nodes of the first set be already placed. In most cases, a large percentage of the nodes in the first set will have been placed, but the percentage of placed nodes in the first set does not have to be 100%. The present method is perfectly valid for any percentage down to and including 0%. A second set of nodes from the logic design hierarchy is then selected for placement in the floor plan. The first set of nodes is compared to the second set of nodes (the "target" set) to determine if the sets are sufficiently analogous. In the preferred embodiment, if the number of nodes in each set is the same, and the parent-child relationships of each set are the same, then further processing may continue. If not, different sets of nodes must be selected. If the sets are analogous, then the second set of nodes is automatically placed in the floor plan in a manner analogous to the first set of nodes. Each node in the target set is placed so that its resulting location relative to other nodes in the target set is analogous to the corresponding source node's position relative to the other source nodes. If a source node is constrained to a region instead of being absolutely placed, the corresponding target node will likewise be constrained to a corresponding region. If a particular source leaf node is not explicitly placed, the corresponding target node will remain unplaced.

(Emphasis Added)(Aubel et al., column 7, lines 15-47). As can be seen, Aubel et al. suggest placing a "target" set of nodes in a manner that is analogous to a "source" set of nodes, so long as source and target set of nodes are sufficiently analogous.

The Examiner also references Figure 4 (e.g. step 38 of Figure 4a) of Aubel et al. as suggesting the step of identifying only the source leaf cell that is connected to the selected net. However, step 38 of Figure 4a recites "selecting source nodes in logic hierarchy" (Emphasis Added). However, the term "nodes" referenced in Figure 4a does

not appear to refer to "nets", as defined in claim 1. With reference to Figure 4A and Figure 4B, Aubel et al. state "[a] node in the graph represents a logic function if it has child nodes, or a cell if it does not have child nodes." (Aubel et al., column 11, lines 27-29)(Emphasis Added). Thus, the nodes referenced in Figure 4A and Figure 4B do not appear to be "nets", as defined in claim 1.

In paragraph 8 of the Office Action, the Examiner rejected claims 7 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Varadarajan et al. as applied to claims 1, 23 and 33 above, and further in view of Garnett et al. (U.S. Patent No. 6,516,456). After careful review, Applicants believe that this rejection is improper because Garnett et al. is disqualified as prior art under 35 U.S.C. §103.

Garnett et al was filed on January 27, 1997, and issued on February 4, 2003. The present application was filed on June 20, 2000. As such, Garnett et al. would only qualify as prior art under 35 U.S.C. §102(e). In view thereof, the Examiner's rejection of claims 7 and 29 must have been made under 35 U.S.C. §102(e)/103.

35 U.S.C. § 103(c) states:

> *35 U.S.C. 103. Conditions for patentability; non-obvious subject matter.*
>
> *****
>
> (c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

35 U.S.C. 103(c) applies to all utility, design and plant patent applications filed on or after November 29, 1999, which includes the present application. The subject matter of

U.S. Patent No. 6,516,456 to Garnett et al. and the subject matter of the present application were, at the time the invention was made, owned by or subject to an obligation of assignment to a common assignee, namely, Unisys Corporation of Blue Bell, PA, U.S.A. In view of the foregoing, Garnett et al. is disqualified as prior art under 35 U.S.C. §103, and for these and other reasons, claims 7 and 29 are believed to be in condition for allowance.

In paragraph 9 of the Office Action, the Examiner rejected claims 8-14 under 35 U.S.C. § 103(a) as being unpatentable over Varadarajan et al. in view of Garnett et al. (U.S. Patent No. 6,516,456) as applied to claim 7 above, and further in view of Aubel et al. As noted above, Garnett et al. is disqualified as prior art under 35 U.S.C. §103. For these and other reasons, claims 8-14 are believed to be in condition for allowance.

In paragraph 10 of the Office Action, the Examiner rejected claims 18, 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Varadarajan et al. in view of Aubel et al. as applied to claim 15 above, and further in view of Garnett et al. As noted above, Garnett et al. is disqualified as prior art under 35 U.S.C. §103. For these and other reasons, claims 18, 21 and 22 are believed to be in condition for allowance.

Finally, in paragraph 11 of the Office Action, the Examiner indicated that claims 30-32 are objected to as being dependent upon a rejected base claim , but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Because the base claim is believed to be in condition for allowance, dependent claims 30-32 are also believed to be in condition for allowance.

In view of the foregoing, it is believed that all pending claims 1-34 are now in condition for allowance. Issuance of a notice of allowance in due course is respectfully

requested. If a telephone conference would be of assistance, please contact the undersigned attorney at 612-677-9050.

Respectfully submitted,

Joseph Peter Kerzman et al.

By their attorney,

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Brian N. Tufte, Reg. No. 38,638
CROMPTON, SEAGER & TUFTE, LLC
1221 Nicollet Avenue, Suite 800
Minneapolis, MN 55403-2402
Telephone: (612) 677-9050
Facsimile: (612) 359-9349